



A detailed cross-sectional diagram of a semiconductor device. The substrate 1 consists of two main layers, 1a and 1b. On top of layer 1a, there is a gate stack 9. To the right of the gate stack, there are source/drain regions 7. Interconnects 11a and 11b are shown at the bottom, with 11a being a horizontal line and 11b being a vertical line. A third interconnect 12 is shown as a horizontal line above the gate stack. Various other components are labeled with numbers like 2, 3, 3a, 3b, 4, and 9d. Two upward-pointing arrows labeled F1 are located at the bottom left and bottom right, indicating forces applied to the substrate or interconnects. A downward-pointing arrow labeled F2 is located at the top center, pointing towards the gate stack.

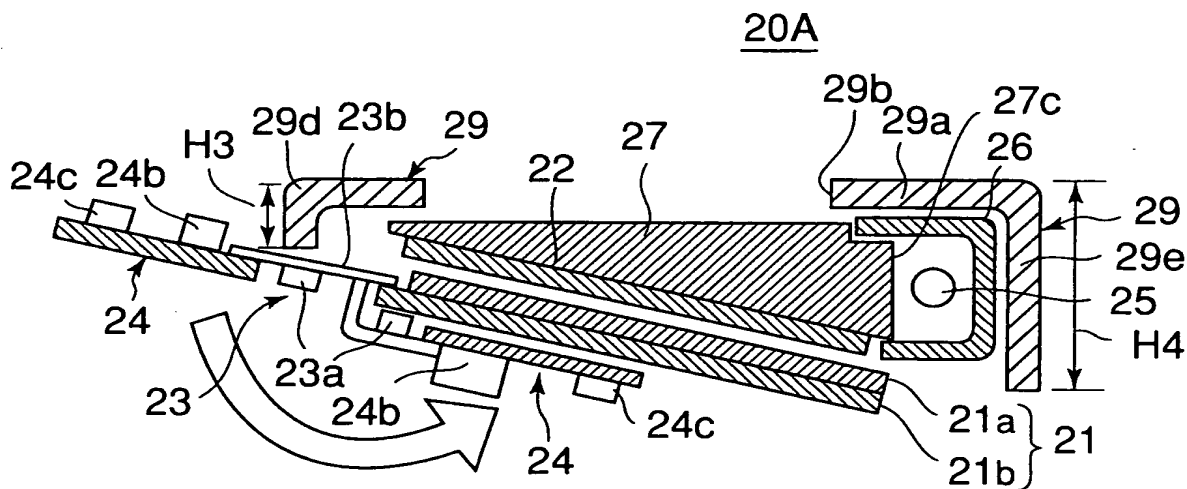


FIG. 7

20B

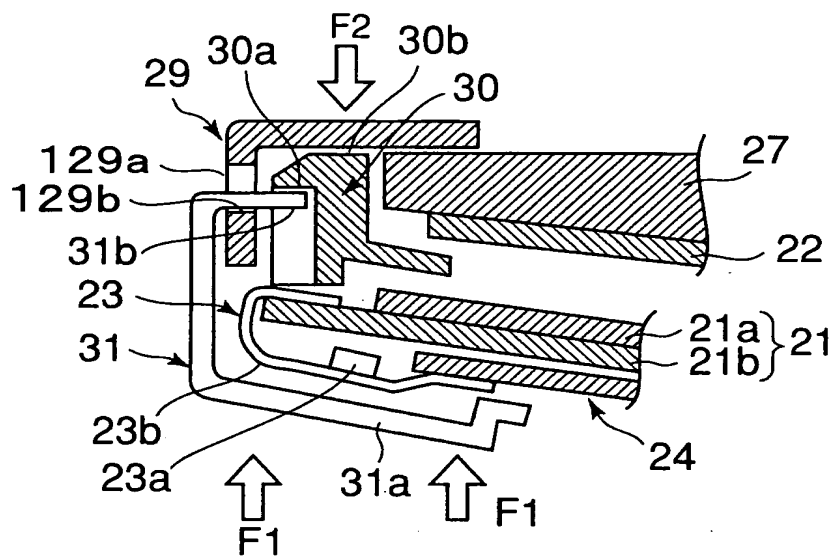


FIG.8

